SPECIFICATIONS

Latched Mode: Dataway signals are handled as follows:

Latched at S1		Latched at S2		Stretched	
Read Lines	R(24)	Initialize	Z	Strobe 1	S1
Write Lines	W(24)	Clear	C	Strobe 2	S2
Function Code	F(5)			Busy	B
Subaddress	A(4)			LAM	L
Station No.	N				
Q Response	Q			(Stretching to	
X Response	X			200 msec	
P1 Bus				provides visual	
P2 Bus				indication.)	

Track Mode: Provides real time continuous display of the dataway signals as well as the ±6 V, ±12 V and ±24 V power lines.

Display: Status of the dataway signals and power supplies is displayed with front-panel LEDs.
Manual Control: A LAM can be generated and the Latched or Track modes selected via front-panel switch.
Computer Control and Readout: Previously latched data and status can be read by a computer. Also, the computer may test and reset the LAM request.
General: Packaging is in conformance with the CAMAC standard for instrumentation modules (IEEE-583). RF-shielded CAMAC #1 width module.
Operating Temperature Range: +15°C to +35°C.
Power Requirements: 1.5 A at +6 V, 50 mA at -6 V, 50 mA at +24 V, 50 mA at -24 V.

CAMAC COMMANDS

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Z or C: All registers, LAM and Lamp Test are cleared by the CAMAC "Clear" or "Initialize" commands.

X: X = 1 for all valid F commands with the appropriate A and N.

Q: A Q = 1 response is generated in recognition of a valid F(0) or F(1) read function or F(8) or F(27) if LAM is set.

L: Look-at-Me signal is generated by pressing the TR/LAM switch on the front panel or sending an F(25) when LAM is enabled.

CAMAC FUNCTION CODES

F(0)•A(0): Read Data: reads the data from the most recently executed CAMAC write operation. The data returned is meaningful only when the Model 2050 is in Latched Mode (TR/LAM switch in center position). The act of reading this register will alter the contents of the Read Data LEDs.

F(0)•A(1): Read Local Timer status word. Bit functions are:

1. True if Timer value exceeds 0.5 of selected time-out period.
2. True if Timer value exceeds selected time-out period.
3,4. Bits indicate time-out periods from 10 msec to 10 seconds.

R4	R3	Time-Out Period
0	0	10 msec
0	1	0.10 sec
1	0	1.0 sec
1	1	10 sec

F(1)•A(0): Read Status: returns the state of the command lines from the previous CAMAC cycle. If LAM is set, it is cleared at S2. For bit assignment see manual. Note: if Bit 14 is true, then the Model 2050 is in Track Mode and bits 1 - 13, 15 and 16 are undefined.

F(1)•A(1): Read Module identification word. Bits 10, 11, 12 and 13 are permanently asserted and bits 1, 2, 3 and 4 are selectable via on board switch. All others are zero.